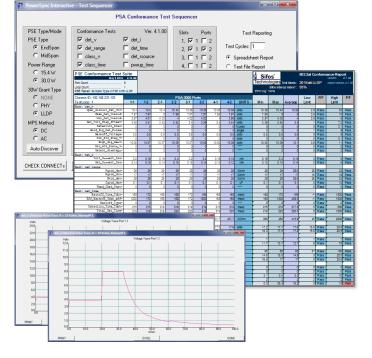


PSA-CT PSE Conformance Test Suite for the PSA-3000 PowerSync® Analyzer

Product Overview





Key Features

- Robust 802.3at (PoE+) PSE Compliance Testing
- □ Fully Automated Port Sequencing and Statistics
- Greater than 95% 802.3at PICS Coverage* from 23 Tests Producing more than 75 IEEE 802.3at Test Parameters per Port
- Fully Emulates All Type-1 (PD Class 0, 1, 2, or 3) and Type-2 (PD Class 4) PD's Including PoE LLDP-Capable PD's
- Adapts to All Prevalent PSE Signaling and Power Behaviors
- Adapts to Prevalent Composite 802.3at and Proprietary Detection Signaling Behaviors
- Configurable Waveform Trace Diagnostic Generation and Retention to 10 Waveforms per Test
- Colorful and Informative Spreadsheet Reporting with Compliance (Pass/Fail) Notations and Parameter Statistics
- Run & Sequence from PSA Interactive GUI or PowerShell PSA Command Line



IEEE 802.3 PSE's

Type-1/Type-2 End-Span Type-1/Type-2 Mid-Span PoE/PoE+ Connectors Power Injectors

The Industry "Norm"

Unmatched 802.3at Specification Coverage Widely Used by PSE Silicon Manufacturers

Fully Automated One-Button Testing

Automatic Adaptation to PSE Probing Techniques and Hybrid-Legacy Probing

Flexibly Sequence Tests and Test Ports

Pop-Up Spreadsheet Reporting with Statistics and Limit Evaluation

Always Up-To-Date

Constantly Enhanced and Improved

Tracking Service Support Agreement

Responsive Support

Overview

Power-over-Ethernet (PoE) challenges design and test engineers to evaluate multi-channel, "smart" DC power sources that are activated and deactivated through signaling protocols operating over several power delivery and polarity configurations. The application and management of DC power over multiple local area network connections must be completely transparent, safe, non-destructive, and non-disruptive to the traditional data transmission behaviors of those network connections and associated network equipment.

Higher Power with 802.3at

Under the IEEE 802.3at standard, power delivered to a single Powered Device is effectively doubled to 25.5 watts. PSE's will pack more electrical power and more processing power to manage that electrical power. Issues of safety and specification compliance are accentuated by the higher power delivery capabilities of each Ethernet Port.

Smarter PSE's and PD's

In the newer 802.3at realm, end-span PSE's such as data switches and routers can use Link Layer Discovery Protocol (LLDP) to communicate power needs and availability with a new generation of Powered Devices (PD's). This extended protocol is a core component of PSE power resource management with granularity to 0.1 watt per Ethernet port.

Fully Automated Testing with Very High Test Coverage

The PSE Conformance Test Suite for 802.3at produces between 75 and 112 IEEE 802.3at test parameters per PSE port depending upon PSE capabilities. These parameters are measured in 23 distinct tests that may be selected and sequenced across up to 24 PSE ports at a time. The test covers over 95% of the PSE PICS (conformance check list items) in the IEEE 802.3at specification*. The PSE Conformance Test Suite is widely used throughout the internetworking community as the industry "norm" for PSE specification compliance.

Flexible PD and LLDP Emulation

The 802.3at standard, unlike its 802.3af predecessor, allows for a variety of PSE and PD types including higher power PD's and LLDP-capable PSE's and PD's. As a result, PSE Conformance Testing now requires increased test "cases" to allow for the variety of powering configurations that can arise. The PSE Conformance Test Suite for 802.3at enables each of these test cases so as to assure full test coverage of all PSE types.

Robust Diagnostics and Reporting

The PSE Conformance Test Suite for 802.3at can automatically sequence to a pop-up spreadsheet report with full color notations of parameter pass/fail status per port and cross-port statistics for each parameter. This report automatically adapts test limits to the test case that is sequenced. Many of the PSE Conformance Tests capture and analyze various voltage and load current "scope" traces in order to evaluate measurement parameters. These traces can be automatically posted to the display, accumulated, and retained until the end of each test for diagnostic purposes. Each trace is individually notated with a description of the trace purpose or measurement parameter.

* For 802.3at PICS Coverage, see Sifos application note: 802.3at PSE PICS Coverage.pdf



PSE Conformance Tests & Parameters

Detection Probing and Functional Tests

det_v	Detection Pulse Waveform Parameters							
	Captures and analyzes F signatures.	PSE detection probe voltages with both valid and slightly non-valid detection						
	Voc	Peak open circuit (disconnected) detection voltage						
	Vvalid(Max)	Maximum Detection Step Level with Valid Signature						
	Vvalid(Min)	Minimum Detection Step Level with Valid Signature						
	∆Vtest	Detection Step Magnitude						
	Detection Slew	Detection step slew rate						
	Good_Sig_Det_Pulse	Number of Detection Signal transitions						
	Vbkoff	Minimum Voltage during detection (ALT B) backoff						
	Non802_Step_V	Level of any pre-detection signals						
	High_Sig_MaxV	Maximum detection voltage with high detection signature						
	Non802_Discr?	Dependence upon Non-802 detection for validity. PSE's that use non-802.3 detection measurements to resolve a valid signature band will report "1".						
	Detect Strategy	Reports PSE Detection as one of five known strategies including 802.3at standard, proprietary pre-detection, etc.						
det_i	Detection Current	Limiting						
	Measures maximum cur	rent sourcing capability from a PSE during detection.						
	lsc(Init)	Max detection current at minimum detection voltage						
	Isc(Det)	Max detection current during detection						
det_range	Detection Passive Acceptance Range							
	Assesses the range of acceptable PD signatures and the reliability of valid detection given random connect timing and capacitive loading.							
	Rgood_Max	Maximum accepted detection resistance signature						
	Rgood_Min	Minimum accepted detection resistance signature						
	Rmid_det	MAX (or MIN) detection resistance given random connections						
	Cgood_Max	Maximum accepted detection capacitance signature						
	Rbad_Cbad_Stat	Power-Up status given a 35Kohm (marginally high) resistive signature with the lowest Capacitive signature rejected by the PSE.						
det_time	Detection Timing							
	Measures detection back	koff and detection probe timing parameters.						
	Tdbo	Detection back-off time (between failed detections)						
	Tdbo_eff	Effective back-off time for PSE's that ignore rather than disable detection measurements						
	Tdet	802.3at detection time duration						
	Tdet_tot	Total detection time including pre-detection measurements						
	Backoff_Type	Reports PSE Detection back-off as one of several known strategies including 802.3at standard, legacy, and 4-pair detection schemes						
det_rsource	PSE Output Resist	ance during Detection						
	Measures effective source	ce resistance of PSE port during detection.						
	Zout	PSE estimated output impedance during detection						
Classification Signaling and Functional Tests								

Classification Voltages class_v

Captures and analyzes F prior to power-up.	PSE classification voltage levels, focusing on only the final classification performed
Vclass	Class Pulse Average Voltage with 1 mA class signature
Vclass_min	Class Pulse Average Voltage with 45 mA class signature
Vmark	Mark Region Voltage with 4 mA mark signature load
Vmark_min	Minimum Port Voltage measured over both MARK regions until power-up

Classificati	ion Signaling and	d Functional Tests							
class_time	Classification Tim	ing							
	Captures and analyzes F prior to power-up.	PSE classification signal timing, focusing on only the final classification performed							
	Event_Count	Count of class pulses							
	Tpdc	Duration of class pulse given Single-Event Classification							
	Tcle1	Duration of first class pulse given 2-Event Classification							
	Tcle2	Duration of second class pulse given 2-Event Classification							
	Tme1	Duration of first mark interval given 2-Event Classification							
	Tme2	Duration from end of second class pulse to power-up given 2-Event Classification							
class_err	Classification Curr	rent Limiting							
		niting applied to classification signals by PSE as well as PSE powering behaviors llegal classification signatures.							
	Class_lim	Maximum Class Current before PSE starts to limit Class Current							
	Vport_CL_lim	Power-Up response (as Port Voltage) following a current limited classification							
	Vport_CL_err_1	Power-Up response (as Port Voltage) following a 55mA (invalid) classification load							
	Mark_lim	Minimum Mark Current Supported during 2-event Mark Region - tested at 5.5 mA and 105 mA given 2-Event Classification							
	Vport_CL_err_2	Power-Up response (as Port Voltage) following up to 3 successive class signatures that changed from Event #1 to Event #2 (asymmetrical signature)							
	Treset	Duration of PSE IDLE state following asymmetrical class signature							
class_lldp	LLDP Protocol and	d Mutual Discovery Testing							
	Assesses PSE LLDP basic protocol fields, protocol timing, and power request processing for both Type-1 and Type-2 PD's.								
	PSE_Source_Priority	Bit Field for PSE Source, Priority, Reserved							
	PSE_MDI_Pwr_Sup	Bit Field from legacy TLV for Port Class, MDI Power Support, MDI Power State, Pair Selection, and Reserved							
	PSE_LLDP_Time_1	Time from Power-ON state until first PoE LLDP frame from PSE given Type-1 PD							
	PSE_LLDP_Type_1	PSE Type advertised by a PSE given Class 0-3 PD signature							
	PSE_Echo_Time_1	Time for PSE to echo back the PD Requested Power level							
	PSE_Alloc_Pwr_1	Allocated Power in response to 8.1 W PD Request from a Class 0–3 PD							
	PSE_Alloc_Time_1	Time to respond To 8.1 W PD Request with Power Allocated							
	PD_Power_Adjust_1	Allocated Power in response to a Change Request from 8.1W to 13W							
	PSE_Adjust_Time_1	Time to echo a PD 13 watt PD Change Request							
	PSE_LLDP_Time_2	Time from Power-ON state until first PoE LLDP frame from PSE given Type-2 PD							
	PSE_LLDP_Type_2	PSE Type advertised by PSE given Class 4 PD signature							
	PSE_Echo_Time_2	Time for PSE to echo back the PD Requested Power level							
	PSE_Alloc_Pwr_2	Allocated Power in response to 20.3W PD Request from a Class 4 PD							
	PSE_Alloc_Time_2	Time to respond To 20.3 W PD Request with Power Allocated							
	PD_Power_Adjust_2	Allocated Power in response to Change Request from 20.3W to 25.5W							
	PSE_Adjust_Time_2	Time to echo a PD 25.5 watt PD Change Request							

Power-Up Processes

pwrup_time	Power-Up Timing Parameters						
	Measures power	r-up rise time and time delay from completion of final detection until power applied.					
	Trise	Rise Time from 10% to 90% of Vport					
	Tpon	Time from end of detection until power-up, Tpon is measured from the final complete detection probe preceding a power-up					
pwrup_inrush	PSE Current	Limiting Behaviors During Power-Up					
		current limiting and inrush overload tolerance parameters. Assures compliance to 3-14, Ilnrush current and timing limits in the POWER_UP state. Maximum output current immediately after 1 msec of a severe inrush overload					

Power-Up Processes

Max_Inrush_c0	Maximum output current in time interval from 1 to 75 msec given Class 0, 1, 2, or 3 PD
Max_Inrush_c4	Maximum output current in time interval from 1 to 75 msec given Class 4 PD
Min_Inrush	Minimum output current while current limiting in time interval from 1 to 50 msec given 30V or higher port voltage
Tinrush	Duration of current limiting until PSE removes power
Inrush_45m	Port voltage after 50msec following 45 msec current limiting inrush overload
Max_Init_Inrush	Maximum output current up to 1 msec given a severe inrush overload
Vinrush	Average Port Voltage - PSE current limiting, PSA foldback suppression applied
Inrush_Strategy	Indicator if PSE uses "legacy_powerup" exception and consequences thereof categorized into one of five possible outcomes

PSE Powered-On Performance and Processes

pwron_v	Powered Port Vo	oltage, Ripple, and Noise
	Measures PSE port D	C and AC voltages in response to minimum and maximum power loads.
	Vport_min_N	Min Port voltage with 0.5 Watt and Pport_Max (PD Class) loading
	Vport_max_N	Max Port voltage with 0.5 Watt and Pport_Max (PD Class) loading
	Vpp_ripple_N	Peak AC Ripple with 0.5 Watt and Pport_Max (PD Class) loading
	Vpp_noise_N	Peak AC Noise with 0.5 Watt and Pport_Max (PD Class) loading
	Vtrans_max_N	Maximum Port Voltage measured during a 5msec load transient from 12mA to Pport_Max / Vport and back.
	Vtrans_min_N	Minimum Port Voltage measured during a 5msec load transient from 12mA to Pport_Max / Vport and back.
pwron_pwrcap	PSE Port Power	Capacity
	Measures the maximu	Im power delivery capability of a PSE port given various PD Classifications and ns.
	Pcon_c0=	Maximum output power from PSE Port given Class 0 PD
	lcon_%_c0=	Maximum static output current relative to 802.3at Icon(Pclass_0)
	Pcon_c1=	Maximum output power from PSE Port given Class 1 PD
	lcon_%_c1=	Maximum static output current relative to 802.3at Icon(Pclass_1)
	Pcon_c2=	Maximum output power from PSE Port given Class 2 PD
	lcon_%_c2=	Maximum static output current relative to 802.3at Icon(Pclass_2)
	Pcon_c3=	Maximum output power from PSE Port given Class 3 PD
	lcon_%_c3=	Maximum static output current relative to 802.3at Icon(Pclass_3)
	Pcon_c4=	Maximum output power from PSE Port given Class 4 PD
	lcon_%_c4=	Maximum static output current relative to 802.3at Icon(Pclass_4)
	Type-2_Enable	Verifies > 450 mA continuously available at 80 msec following 2-event power-up for 2-event, Type-2 PSE's <i>or</i> verifies >450 mA is not available for LLDP capable Type-2 PSE's prior to negotiation
	Pclass_LLDP_22.7	Indicator of PSE ability to deliver Pclass (Icon) given 22.7W power grant
	Pclass_LLDP_24.5	Indicator of PSE ability to deliver Pclass (Icon) given 24.5W power grant
pwron_maxi	PSE Response t	o Maximum Overloads
		evaluates PSE characteristics with respect to the POWER_ON state PI plates in Figure 33-15 of the 802.3at specification.
	llim_Peak	Maximum output current tolerated by PSE in time frame of 8 to 75 msec
	llim_Min_1	Minimum output current up to 50 msec with 402mA load pulse and foldback suppression applied to assure > 30VDC (Type-1 PD emulation)
	Tlim_1	Time to port shutdown in response to 400 mA overload given Type-1 PD
	Vlim_1	Average port voltage coincident with Tlim_1 measurement
	Ilim_Max_1	Maximum output current from 1 to 75 msec given 700mA load pulse and foldback suppression active given a Type-1 PD
	llim_Low_V_Tol_1	Measures time-to-port-foldback given a Type-1 PD with extreme overload
	Ktran_lo_1	% excursion below 50V given 250usec (fast) overload transient (401 mA) given a Type-1 PD (Type-2 PSE's only)
	llim_Min_2	Minimum output current up to 50 msec with 686mA load pulse and foldback suppression applied to assure > 30VDC given Type-2 PD emulation
	Tlim_2	Time to port shutdown in response to 684 mA overload given Type-2 PD

PSE Powered-On Performance and Processes

	Vlim_2	Average port voltage coincident with Tlim_2 measurement
	llim_Max_2	Maximum output current from 1 to 75 msec given 860mA load pulse and foldback suppression active given a Type-1 PD
	llim_Low_V_Tol_2	Essentially a measure of time-to-port-foldback given a Type-2 PD
	Ktran_lo_2	% excursion below 50V given 250usec (fast) overload transient (686 mA) given a Type-2 PD
pwron_overId	PSE Response	to Maximum PD Power Transients
		est assesses powered PSE port behaviors with respect to Ipeak, the maximum wed to a PD as defined in Equation 33-4 of the 802.3at standard. Percent of required Ipeak current that is supported over 50msec duration where Ipeak required is defined by Equation 33-4 given a Type-N PD – maximum level verified is 125%
	Vport_lpeak_N	Min Port Voltage at Ipeak transient pulse given a Type-N PD
	Vport_5%DC_N	Min Port Voltage over 5 seconds with a quantity of 50 msec Ipeak pulse transients separated by 1 second (5% duty cycle) given a Type-N PD
MPS Processes	s for Power Re	moval on PD Disconnect
mps_ac_pwrdn	Power Timing	and Load Current Impact on AC MPS PSE's
	Evaluates power re	moval timing and DC load tolerance on an AC MPS PSE.

	Evaluates power removal	timing and DC load tolerance on an AC MPS PSE.						
	Tmpdo	Disconnect power-down timing from disconnect event						
	I_hold_ac	Maximum DC Load Current tolerated with AC MPS Disconnect Shutdo						
mps_ac_vf	AC MPS Signaling	Characteristics						
	Measures AC MPS signa V_open V_open_%Vport Fp AC_MPS_SR Isac	ling characteristics during the Tmpdo interval. Peak-Peak AC probing voltage following PD Disconnect Peak-Peak AC probing voltage expressed as a % Vport_pse AC probing signal frequency following PD Disconnect AC probing signal slew rate Signal current sourced by AC MPS signal generation resource						
mps_ac_voff	AC MPS Peak Voltage Characteristics							
	Measures voltage peaks V_open1 Vopen_pk	following PD disconnect and power-down events given an AC MPS PSE. Peak port voltage found after AC MPS power removal event Peak port voltage following PD disconnect over a period of one second						
mps_dc_valid	DC MPS Valid Sign	ature Timing Characteristics						
	Measures intermittent loa Tmps Duty_Cycle_tol	d tolerance thresholds of a DC MPS PSE. Minimum valid signature ACTIVE time required for DC MPS validity PSE power response to valid / invalid load cycling of 16.7% duty cycle						
mps_dc_pwrdn	Power Timing and Threshold Assessment on DC MPS PSE's							
	Evaluates power removal timing and DC load requirements on a DC MPS PSE.							
	l_hold	Minimum current required to maintain power given DC MPS PSE						
	Tmpdo	Disconnect power-down timing from start of invalid signature						
	Vopen_pk	Peak port voltage following PD disconnect over a period of one second						

PSE Power-Down Characteristics

pwrdn_overld	PSE Response	to Non-Current Limiting Overloads
		dling of non-current limiting overloads in the PSE discretionary region of the PI mplates in Figure 33-15 of the 802.3at specification.
	lcut_N	Smallest load current of duration equal to Tcut_Max, or 75 msec, that causes immediate or delayed power removal given a Type-N (1 or 2) PSE.
	Tcut_N	Time from start of transient until power removal but not exceeding 75msec, the duration of the applied load transient.
	lsoft_N	Smallest load current of duration equal to 2 seconds that causes immediate or delayed power removal given a Type-N (1 or 2) PSE.
	Tsoft_N	Time from start of transient until power removal but not exceeding 2 seconds, the duration of the applied load transient.

pwrdn_time	AC MPS Signaling Characteristics						
	Evaluates PSE	disconnect discharge timing as well as output characteristics during power removal.					
	Toff	Power discharge time with hypothetical 320K Ω load.					
	Cout	PSE output capacitance during power discharge					
	Rp	PSE shunt output resistance during power discharge					
pwrdn_v	AC MPS Pea	ak Voltage Characteristics					
	Measures PSE	post-power-removal characteristics following an overload shutdown condition.					
	Voff	IDLE state voltage between detections after overload shutdown					
	Ted	Time from overload condition shutdown until a detection probe leading to a successful power-up					
	Ved	Peak voltage over the Ted interval					

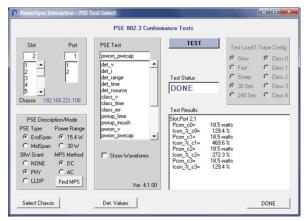
PSE Power-Down Characteristics

Configuring and Running the PSE Conformance Test Suite

The PSE Conformance Test Suite is accessed from either PSA Interactive Software (GUI) or PowerShell PSA, an extended Tcl/Tk command line shell. PSA Interactive provides two menus with access to the PSE Conformance Test Suite: The **PSE Tests** menu and the **Sequencer** menu.

Within each of these menus, users perform 3 declarations* that affect testing and test options:

- PD Emulation: Type-1 (15.4W) or Type-2 (30W)
- PD 30W Grant Type: NONE (Type-1 PSE), PHY (Type-2 2-Event PSE), or LLDP (Type-2 LLDP)
- PSE Disconnect Detection Method: AC MPS or DC MPS



PSA Interactive PSE Tests Menu

User's may also select one of several reporting options, the most common of which will produce a pop-up (Microsoft Excel) spreadsheet report that performs all test parameter limit checking and analysis.

Multi-Port PSE connections can rapidly be verified prior to testing from this menu and as with the PSE Tests menu, users may opt to have waveform traces produced by each test appear on screen as each test runs. Users may also choose to have the sequence terminate as soon as an error condition develops in any test on any port.

The **PSE Tests** menu is geared to running a single test at a time and capturing results from that test. The menu allows users to select a particular PSA test port (slot and port) and then execute a test. Users may optionally select to have any and all measurement waveforms that are used by a given test captured, labeled, and displayed as the test runs.

The **PSE Tests** menu also provides access to certain other specialized testing functions that include user specified loading profiles and LLDP traces.

The **Sequencer** menu allows users to select one or more tests that are to be automatically sequenced along with the PSA test ports that will also be sequenced.

	Р	SA Conformance Test	Sequencer	
PSE Type/Mode PSE Type C EndSpan C MidSpan Power Range C 15.4 W C 30.0 W 300 Grant Type C NONE C PHY C LIDP MPS Method C D C	Conformance Tests Conformance Tests det_range class_v class_time class_time class_time class_time prom_maxis prom_procept prom_proced prom_proced prom_top	Ver. 41.00	Slots Ports 1 7 1 2 2 7 1 7 2 3 7 1 7 2 4 1 1 2 2 5 7 1 7 2 6 1 7 2 2 8 1 7 2 2 9 1 1 2 2 10 1 7 2 1 12 1 1 1 2 12 1 1 7 2	Test Reporting Test Quels: 1 C Spreadheet Report C Test File Report C Standard Time-Date File C User Specified File Enter File Name: paa_report_data.cs Sequence Status
C AC Auto-Discover	T All Tests	Halt on Test Error Show Waveforms	T All Ports	

PSA Interactive Sequencer Menu

* A fourth declaration of **EndSpan** and **MidSpan** does not affect testing.

The PSE Conformance Test Suite Standard Report

The standard spreadsheet test report for the PSE Conformance Test Suite provides efficient feedback by clearly notating any specification compliance violations both by test parameter and by test (PSE) port. The report also accumulates minimum, maximum, and average parameter values across PSE ports so that users can spot

individual port deviations and assess performance to design goals. Multiple cycles of testing can be specified to produce one report page per sequence cycle.

All test limit processing automatically adapts to the mode of PD Emulation, the type of PSE (e.g. Type-1 or Type-2), and other factors that are specified before the sequence begins. Test limit tables are found on the **Limits** page of the report.

The report includes a **Notes** page with detailed explanations of each parameter of each test and an **Interop** page that rates the "Interop" Risks of any particular combination of specification violations.

The report will automatically scaled to the number of tested PSE ports.

PSE Conformance Test S										Sif	05		802.3at C	onform	ance Repo	
May 8 2015 Port Count													30 Watt L	np	version report versio	4.1.0
Loop Count.										reomine		op Index*:			report versit	xi 4. i.i
PSE Tested: Sample Type-2 PSE with										Error Log:	None	op muex .				
Chassis ID: 192.168.221.103				DS	A-3000 F	lorte							Low	P/F	High	P/F
TestLoop: 1	1-1	1-2	2.1	2.2	3-1	3-2	4-1	4-2	UNITS	Min	Max	Average	Limit	P/F	Limit	P/F
Test: det v		1.4			0-1	5-2	4-1		UNITO		mus	Arciugo	Linit		Cinic	
Open_Circuit_Det_Voc=	10.4	10.4	10.4	10.43	10.38	10.38	10.38	10.38	volts	10.38	10.43	10.39	2.8	Pass	30	Pas
Peak_Det_Vvalid=	7.97	7.97	8	7.98	7.97	7.97	7.95	7.97	volts	7.95	8	8	3.8	Pass	10	Pas
Min_Det_Vvalid=	3.97	4.01	4.03	4	4.02	4.02	4	3.98		3.97	4.03			Pass	9	Pas
Det_Volt_Step_dVtest=	3.45	3.41	3.42	3.42	3.4	3.39	3.4	3.44		3.39	3.45	3.4		Pass	7.2	Pa
Detection_Slew=	0	0	0	0	0	0	0	0	V/usec edges	0				Pass Pass	0.1	
Good_Sig_Det_Fulse= Backoff_Voltage=	0.5	0.5	0.6		0.6	0.6	0.6	0.5		0.5				Pass	9	
Non_802_Step_V=	0.0	0.5	0.0	0.5	0.0	0.0	0.0	0.0		0.0				Pass	0.1	
High_Sig_MaxV=	10.05	10.07	10.07	10.09	10.07	10.08	10.05	10.08		10.05				Pass	11	
Non_802_Discr_?=	0	0	0	0	0	0	0	0		0	0			Pass	0	
Detect_Strategy=	0	0	0	0	0	0	0	0		0	0	0	0	Pass	2	Pa
Test: det i																
Init_Current_Isc=	0.2	0.19	0.19	0.2	0.2	0.2	0.18	0.18	mA	0.18		0.19		Pass	5	Pas
Det Current Isc=	0.14	0.15	0.14	0.15	0.15	0.14	0.13	0.12	mA	0.12	0.15	0.14	0	Pass	5	Pa
Test: det range Rgood_Max=	29	29	29	29	28	29	28	28	Kohm	28	29	28.6	28	Pass	32	Pa
Rgood_Max- Rgood_Min=	25	17	17	17	17	25	17	17	Kohm	17	17	20.0	18	Pass	19	
Rmid det=	29	29	29	29	28	29	28	28	Kohm	28	29	28.6		Pass	33	
Cgood_Max=	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1		Pass	10	
Rbad Chad Stat=	0	0	0	0	0	0	0	0		0	0	0	0	Pass	0	Pa
Test: det time																
Backoff_Time_Tdbo=	168	172	168	168	172	168	168	168	msec	168	172	169	-1	Pass	1500	Pa
Eff_Backoff_Idbo_eff=	1200	172	188	168	172	1300	188	168	msec	168	1300	439.5		Pass	1500	
Backoff_Type=	0 215	215	219	219	0 219	219	215	219	msec	215	219	217.5		Pass Pass	0 500	Pa Pa
Detection_Time_Tdet= Total Det Time=	210	215	219	213	210	219	210	210	msec	210	210	20.5	5	Pass	1000	Pa
Test: det rsource	210	210	210			210	210		111111	210		220.0	Ĭ	1 44 5	1000	
Output Impedance Zout=	450	450	388	409.4	410.6	435.4	401.7	401.7	KOhm	388	450	415.9	45	Pass	2000	Pa:
Test: class v																
Class_Voltage_Vclass=	17.7	17.7	17.6	17.2	17.6	17.6	17.6	17.6	volts	17.2	17.7	17.6		Pass	20.5	Pa
Vclass_Min=	17.5	18.3	17.4	17.1	17.4	17.4	17.4	17.4	volts	16.3	17.5	17.2	15.5	Pass	20.5	Pa
Test: class time				1		1				1	1			-		-
Event_Count= Class_Time_Tpdc=	11.7	13.7	13.7	13.7	11.7	13.6	11.7	11.7		11.7	13.7	12.7	1	Pass Pass	75	Pat
Test: class err	1.67	10.7	13.7	13.7	11.7	13.0	11.7	11.7	msec	11.7	10.7	12.1		1-20-3	//0	Fa
Class_lim=	65	65	65	65	65	65	65	65	mA	65	65	65	51	Pass	100	Pa
Vport_CL_lim=	15.5	14.8	14.8	14.8	14.6	14.8	14.6	15		14.6	15.5	14.9		Pass	20.5	
Vport_CL_err_1=	17	17	16.9	17	18.9	17	18.9	17	V	16.9	17	17	0	Pass	20.5	Pa
Test: class lldp																
PSE_Source_Priority=	0	0	0	0	0	0	0	0		0				Pass	0	Pa
PSE MDI Pwr Sup=	0	0	0	0	0	0	0	0		0				Pass	0	
PSE_LLDP_Time_2=	3.1	3.5	3.1	3.1	3.4	3.4	3.4	3.1	sec	3.1	3.5	3.3		Pass Pass	10	Pa Pa
PSE_LLDP_Type_2= PSE Echo Time 2=	2	5.8	6.2	6.2	34.9	- 2	35.3	0.3		0.3	35.3	16.2		Pass	10	
PSE_Lono_lime_z- PSE Alloc Pwr 2=	20.3	20.3	20.3	20.3	20.3	20.3	20.3	20.3		20.3	20.3	20.3		Pass	25.5	
PSE Alloc Time 2=	7	5.8	6.2	6.2	34.9	34	35.3	0.3	5.90	0.3	35.3	16.2		Pass	30	
PD Power Adjust 2=	25.5	25.5	25.5	25.5	25.5	25.5	25.5	25.5	Watts	25.5	25.5	25.5	25.5	Pass	25.5	Pa
PSE Adjust Time 2=	6.2	6.2	5.8	4.9	7	2	5.8	4.1	sec	2	7	5.3	0	Pass	10	Pa
fest: pwrup time																
Pwr-On_Rise_Time_Trise=	27	31	60	48	31	27	67	64	usec	27	67	44	15		50000	Pa
Power-On_Time_Tpon=	93.8	82	11.7	11.7	11.7	15.6	11.7	11.7	msec	11.7	93.8	31.2	0	Pass	400	Pa
Test: pwrup inrush	430.13	429.25	428.88	430.13	431.63	431.63	430.5	430.38	mA	428.88	431.63	430.3	400	Pass	450	Pa
Init_Iinrush= Max_Iinrush_c4=	430.13	423.20	428.88	430.13	431.03	431.03	430.5	430.38	mA	428.88	431.63	430.3		Pass	400	Pa
Min_linrush=	429	428.25	427.25	427.75	430.25	430	428	428.5	mA	427.25	430.25	428.0		Pass	450	Pa
Tinrush=	59.2	59.2	59.2	59.2	58.8	59.2	58	58.4	msec	58		58.9		Pass	75	
Inrush_45m=	54.6	54.7	54.7	54.7	54.6	54.7	54.7	54.7		54.6	54.7	54.7	50	Pass	57	Pa
Inrush_Voltage=	31.8	31.7	31.7	31.7	31.7	31.8	35.7	35.4		31.7	35.7	32.7	30	Pass	57	Pa
Max_Init_Inrush=	503.8	503.5	502.3	504.3	503.8	505.5	714	715	mA	502.3	715	558.5	0	Pass	2000	
Inrush_Strategy_c4=	0	0	0	0	0	0	0	0		0	0	0	0	Pass	1	Pa
fest: pwron v	53.6	53.7	53.8	53.8	53.7	53.8	53.8	53.8	v	53.6	53.8	53.8	50	Pass	57	P-
Vport min 2= Vport max 2=	54.9	53.7	55	53.8	53.7	53.8	53.8	54.9	V	54.8	55	54.9		Pass	57	Pa Pa
Vport_Hax_2= Vport_ripple_2=	180	180	183	183	181	180	202	191	mVpp	180	202	185	0	Pass	500	
		173	172	184	172	172	158	151		152	184	169.8			200	

PSE Conformance Test Suite Standard Report (excerpt)

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